Academic Year: 2017-2018(Ongoing)

UG Projects:

Domain	S.No	Name of the Student	Guide Name	Title of the project
Analog and Mixed IC Design	1	Indhu.B Mohamed Nivas.K	Ms.C.Suganya, AP/ECE	ASIC design of dual quality 4:2 compressors for Vedic multiplier
	2	Deepak Prasad.U Indhumathi.S Priyadharshini G	Mr.B.Pradeep Kumar, AP/ECE	ASIC design of temperature compatible CMOS Adder for Space application
	3	Kavin.D Gogula Krishnan.S Pavithra.R Gowtham. K	Dr.R.Sudhakar, Professor/ECE	ASIC Implementation of binary/decimal floating point fused multiply add(FMA)unit
	4	Karthik.R Keerthana.M Varshinee.V.S Gajendrakumar.S	Ms.C.Kalamani, AP/ECE	ASIC implementation of energy efficient approximate multiplier for DIP application
	5	Priyadharshini.B Deepa.T Akshaya.V.S Keerthi.S	Ms.S.Kalaiselvi, AP/ECE	ASIC Implementation of Energy Efficient Inexact Radix-8 Booth Multiplier
	6	Saranya.S Geethapriya.S Gowtham.K	Ms.P.Sathyabama, AP/ECE	ASIC implementation of fault tolerant XOR/XNOR based full adder for image processing applications.
	7	Santhosh Kumar.M Vishnu.V Mahesh Kumar.S	Dr.K.N.Vijeyakumar, Asso.Prof./ECE	CMOS Design Of Low Noise Amplifier For Satellite Communication and Bluetooth Receiver
	8	Vigneshwar.M Ragunath.R	Dr.K.N.Vijeyakumar, Asso.Prof./ECE	ASIC Implementation of R-2R Digital to Analog Conversion
	9	Abishek Karthick.V Krishnamoorthi.K Anitha.S	Ms.C.Kalamani AP/ECE	Design and implementation of low noise and high gain Gilbert mixer for transceiver
	10	Kanchana.S Naveen,J	Ms.C.Suganya AP/ECE	VLSI Implementation of Image

		Anusuya Devi.I		Enhancement Algorithm for Image Processing Applications
	11	Vijayalakshmi.K	Ms.S.Kalaiselvi AP/ECE	ASIC Implementation of approximate voting scheme for reliable computing
	12	Malar Vizhi.S	Dr.K.N.Vijeyakumar, Asso.Prof./ECE	ASIC Implementation of DIT-FFT Butterfly Architecture Using Approximate Units
Digital IC Design	1	Annal Mahizhini.R Dinesh kumar.R Hari Narayan.B	Dr.K.N.Vijeyakumar, Asso.Prof./ECE	Design of Floating point ALU using Reversible logic gate
	2	Keerthigaa.T Saranyaa.T Gowthami. D Ganaga Rajesh .G	Dr.K.N.Vijeyakumar, Asso.Prof./ECE	VLSI implementation of high speed low power circuit for factorial calculation using ancient vedic mathematics
FPGA Implementation of Image and Signal Processing Applications	1	Vinoth Kumar.T Sriram.K Jeya Prabu.K Divya.K.P	Mr.Kathirvel AP/ICE	High performance Significance Approximation Error Tolerance Adder for Image Processing Applications.
	2	Nithya.A Sudha.B Mohan.R Ganesh kumar	Mr.GopalKrishnan AP/EIE	High Speed Energy Efficient Static Segment Adder For Approximate Computing Applications

PG Projects:

Domain	S.No	Name of the Student	Guide Name	Title of the project
Analog and Mixed IC Design	1	Arunthathi.G	Dr.K.Umamaheswari AP/EEE	VLSI Design of Serializer for 12Gbps
	2	Kavya Dharshini.S	Mr.A.Nandhakumar AP/EEE	VLSI Design of De-serializer for 12Gbps
Digital IC Design	1	Sindhu.L	Dr.K.Sumathi Asso.Prof./ECE	VLSI architecture for Image Compression using Haar Wavelet Transform
	2	Sasikala.C	Dr.K.N.Vijeyakumar, Asso.Prof./ECE	VLSI Architecture for DIT-FFT algorithm for OFDM Applications
	3	Gayathri.S	Dr.A.Senthil Kumar	VLSI Implementation

			Professor/EEE	of Water Marking Algorithm Using Phase Congruency and Singular Value Decomposition
	4	Hema.P	Ms.K.Saranya AP/EEE	ASIC Implementation of Signed Multiplier using Compressor
	5	Jayasurya.K	Ms.M.Sangeetha, AP/EEE	VLSI Implementation of Reduced Size Array Multiplier
FPGA Implementation of Image and Signal Processing Applications	1	Sangavi.K.B	Dr.R.Sudhakar Professor/ECE	Development of VLSI Architecture for removal of Impulse Noise
	2	Brindha.T	Dr.B.Vinoth Kumar AP/EEE	VLSI Implementation of High Speed Architecture for Adaptive Median Filter